WEST Search History

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DATE: Monday, November 07, 2005

Hide?	Set Name	Query	Hit Count
		DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ	
☐	L10	L9 and @AD<20010316	3
☐	L9	(change or replace or changing or replacing) near5 ((control character) or K28.5) near5 ((data character) or D28.5)	6
☐	L8	L6 and ((change or replace or changing or replacing) near5 character)	1
☐	L7	L6 and l3	0
☐	L6	encapsulation same decapsulation	426
☐	L5	L4 and @AD<20010316	0
☐	L4	K28.5 same D28.5	6
☐	L3	L2 and @AD<20010316	6
☐	L2	(FC or (fiber channel)) same (control character) same (data character)	13
☐	L1	(FC or (fiber channel)) same (control character)	97

END OF SEARCH HISTORY

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L3: Entry 3 of 6 File: USPT Sep 15, 1998

DOCUMENT-IDENTIFIER: US 5809341 A
** See image for Certificate of Correction **
TITLE: Circuit for transmitting received character when detection signal is not activated and transmitting substitute character when the detection signal is activated

Application Filing Date (1):
19960628

Detailed Description Text (37):
To transmit data in Async-HDLC with transparency mapping, the transmitter circuit 800 includes transmitter (Tx) mapping logic 802, which receives data (i.e., address, control, and information fields) and FCS (i.e., FCS fields) characters to be transmitted from a parallel MUX circuit 807, which in turn, receives the data characters from the FIFO memory 402' through the P/S circuit 606 and the FCS characters corresponding to the data characters from the FCS generator circuit 608. Since the Tx mapping logic 802 treats both the data and FCS characters in the same fashion, both are simply referred to herein for convenience, as "characters". The order in which the data and FCS characters are received by the Tx mapping logic 802 is the same as described in reference to the parallel MUX circuit 628 of FIG. 6. The Tx mapping logic 802 is enabled through a map enable signal ME provided, for example, by the TX control circuit 804 or the local processor 114 of the transmitting computer system 100. Active ones of a set of control characters to be mapped are indicated by a plurality of control character enable signals TxCCEN deriving from, for example, a transmitter (Tx) ACCM register. After processing each received character, the Tx mapping logic 802 provides its output to a first set of inputs of a parallel MUX circuit 810, which is also provided at respective second and third sets of inputs, a flag byte, hex 7E, from the flag byte register 612, and a control character from a transmitter (Tx) control character (C--C) register 809. The parallel MUX circuit 810 passes a character provided at any one of its first, second or third sets of inputs to its output, as determined by input select signals SEL6 provided, for example, by the TX control circuit 804 or the local processor 114 of the transmitting computer system 100, to a parallel-to-serial (P/S) circuit 620 which serially passes each parallel received character to the remainder of the asynchronous data path 803 to be transmitted in the Async-HDLC with transparency mapping format through the serial communication channel 136.

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